NXTON

XT2114A

Isolated PSR Controller

Features

- Primary side constant current Regulator
- Input AC line Over voltage protection
- Input AC line Under voltage protection
- THD optimize for wide input AC range
- Current foldback with high temperature
- Quasi-resonant mode (QRM)
- Very fewer external components
- Programmable input line voltage ompensation
- Leading edge blanking for CS/FB pin
- Provides Protection Functions
  - Over-Temperature Protection with hysteresis
  - VDD Over Voltage Protection
  - CS pin cycle by cycle current limit
  - Output Short Circuit Protection
 - Output Over Voltage Protection

Applications

- LED Lighting
- Constant Voltage and Constant Current Regulation

Description

XT2114A is a high-power factor, high constant current precision and high efficiency primary side controller, which build in input AC line over voltage/under voltage protection and output current foldback under high ambient temperature. It supports both isolated fly-back and non-isolated Buck-Boost application. XT2114A introduces advanced primary constant current control tec nology and then the secondary output current is controlled well by primary side information wit out extra optocoupler, which simplify the secondary side control circuit greatly. The unique four levels output current foldback value under high ambient temperature is selectable only by one external resistor. XT2114A operates in Quasi resonant mode, which can reduce the switching loss of MOSFET. With optimized valley detection and line voltage compensation circuit, it ensures the output current accuracy under the universal input AC voltage range. Meanwhile, the leading-edge blanking circuit on CS and FB pins enhances the anti-noise ability of the system wit out additional filter co ponents. XT2114A has complete protection function, auxiliary winding over-voltage protection, VDD secondary overvoltage tion, output short circuit ion, cycle-by-cycle current limiting and auto restart after protect occur.

Typical Application

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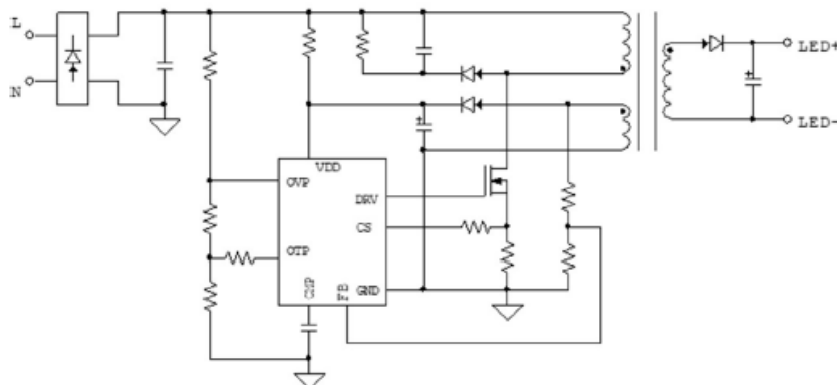
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PIN DIAGRAM（SOP8）

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CMP  1        8  OVP
FB   2        7  OTP
CS   3        6  VDD
GND  4        5  DRV
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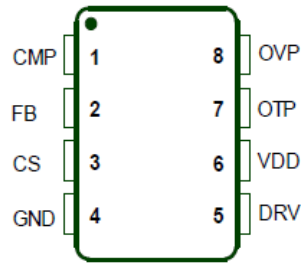
ABSOLUTE MAXIMUM RATTINGS (Note 1)

| Parameter	Value	Unit
VDD and DRV	30	V
CMP, FB, CS, OVP and OTP	0.3V to 6.5	V
Thermal Impedance, θJA SOP8	165	°C/W
Junction Temperature	160	°C
Soldering Temperature (10 sec.)	260	°C
Storage Temperature Range	-55°C to 150	°C
ESD Capability (Note2) HBM		
HBM	2	KV
MM	200	V
RECOMMENDED OPERATING RANGE (Note3)		
Junction temperature	-40 to 150	°C
Ambient temperature	-40 to 85	°C
VDD Supply Voltage	11 to 23	V
VDD capacitance value	2.2 to 22	uF

Note 1, the "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed and may cause permanent damage to the XT2114A. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the Electrical Characteristics section of the specification is not implied. The "Electrical Character-istics" table defines the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability

Note 2, It is sensitive for ESD case, some preventive measures are recommended.

Note 3, Not guaranteed if operated outside recommended operating range.

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BLOCK DIAGRAM
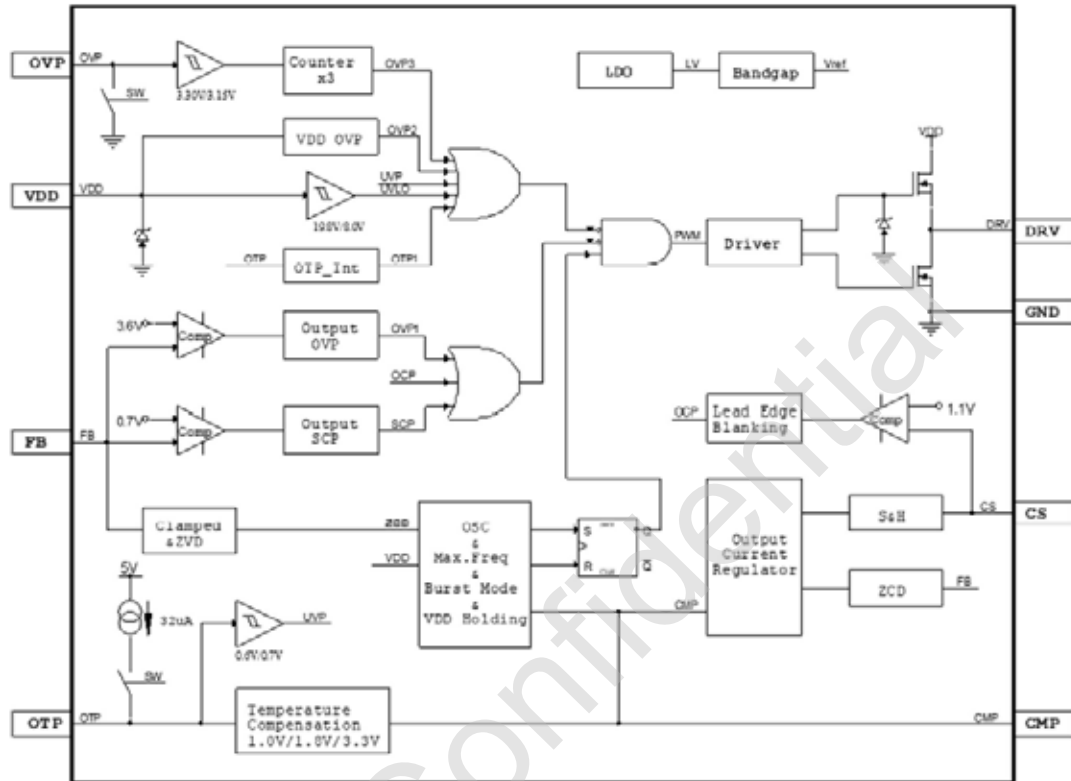
PIN DESCRIPTION

Name	I/O	Pin No.	Description
CMP	I	1	Loop Compensation, OTA output, Connect external RC to GND
FB	I/O	2	Zero current detection, Output Over Voltage Protection and input AC line Voltage compensation
CS	I	3	Current Sense
GND	POWER	4	Power GND
DRV	O	5	Drive External MOSFET, Clamped maximal 16V in Controlle
VDD	POWER	6	Controller Power Supply
OTP	I	7	Output current foldback setting with ambient temperature Input AC line under voltage protection setting
OVP	I	8	Input AC line Over Voltage Protection setting

ELECTRICAL CHARACTERISTICS (NOTE4)

（VDD=15V, TA=25℃ unless otherwise noted.）

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
VDD（Pin6）						
I_{ST}	Startup VDD Current	VDD=VDD$_{ON}$ 0.3V		5	10	μA
I_{OP}	Operation VDD Current	C_{DRV}=1.5nF		1.5		mA
VDD$_{ON}$	VDD Turn-on Threshold Voltage		18.1	19.8	21.5	V
VDD$_{OFF}$	VDD Turn-off Threshold Voltage		7.0	8.0	9.0	V
VDD$_{OVP}$	VDD Over Voltage Protection			27		V
CMP（Pin1）						
V_{REF}	OTA reference voltage		247.5	253.0	258.5	mV
I_{CMP_SINK}	CMP maximal sink current			106.6		uA
I_{CMP_SOURCE}	CMP maximal source current			16		uA
V_{CMP_MAX}	CMP high clamped voltage			3.6		V
FB（Pin2）						
V_{FB_SINK}	FB high clamped voltage	2mA sink current		6		V
V_{FB_SOURCE}	FB clamped source current	4mA source current	-150	0	+150	mV
V_{FB_ZCD}	FB zero voltage detection			0.5		V
V_{FB_OVP}	FB over voltage protection			3.6		V
V_{FB_SCP}	FB short circuit protection			0.7		V
CS（Pin3）						
V_{CS_LIM}	Cycle by Cycle current limit Threshold on CS pin	FB=0V	0.9	1.1	1.3	V
$\Delta I_{CS} / \Delta I_{FB}$	Relationship between CS compensation voltage and FB pin source current	RCS=1kΩ		30		mV/mA
T_{BK_CS}	CS pin Leading edge blanking		300	400	500	nS

OTP （Pin7）							
V_{UVP}	AC line under voltage protection				0.7		V
T_{UVP_ST}	Startup AC line under voltage detection delay time				12		mS
V_{UVP_R}	AC line under voltage protection release voltage				0.6		V
I_{OTP}	OTP source current	$V_{OTP} < 5.0V$			32		uA
T_{OTP_HY}	Release hysteresis temperature after OTP occur				30		°C
I_{DE_RATIO}	Current Drop Rate with temp.				8		%/°C
I_{DE-MIN}	Minimal value after current foldback with high temperature occur				20%		IMAX
T_{ZF1}	Foldback temperature value 1	$V_{OTP} < 1.0V$			128		°C
T_{ZF2}	Foldback temperature value 2	$1.0V < V_{OTP} < 1.8V$			106		°C
T_{ZF3}	Foldback temperature value 3	$1.8V < V_{OTP} < 3.3V$			99		°C
T_{ZF4}	Foldback temperature value 4	$3.3V < V_{OTP}$			90		°C
V_{PRO}	Over temperature protection				155		°C
OVP （Pin8）							
V_{OVP}	Input AC line over voltage protection				3.3		V
V_{OVP_RE}	Release voltage after V_{OVP} occur				3.15		V
T_{OVP_ST}	Startup AC line over voltage detection delay time				12		mS
N_{OVP}	Input AC line OVP delay time				3		CLK
DRV （Pin5）							
T_R	DRV Rising Time	CL=1nF	150	200	220		nS
T_F	DRV Falling Time	CL=1nF	80	100	120		nS
V_{DRV_CLAMP}	DRV max. clamped voltage				16		V
Oscillator							
F_{MAX}	Maximal switching frequency				120		kHz

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T_{MAX_ON}	Maximum on time			15.2	uS
T_{MAX_OFF}	Maximum off time			40	uS
T_{MIN_OFF}	Minimum off time (NOTE5)			10	uS

Note 4: Use of this product outside the limits of the test conditions may experience in a variation of parameters from the published parameters. If additional information is needed, please consult with Nxton

Note 5, After minimal off time, switch turn on again until the valley bottom detection is effective, there is a certain deviation between the design value and actual value.

TYPICAL REFERENCE APPLICATION CIRCUIT (Note 6)
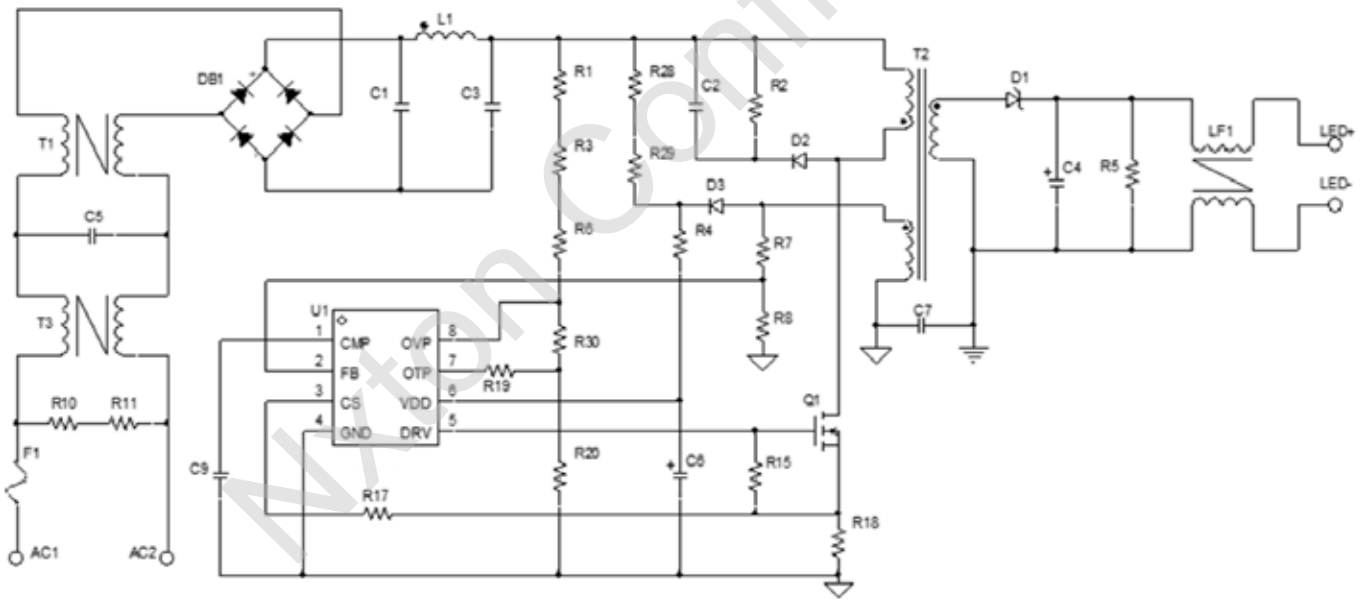
Note6, it is only reference application circuit, not update to the latest.
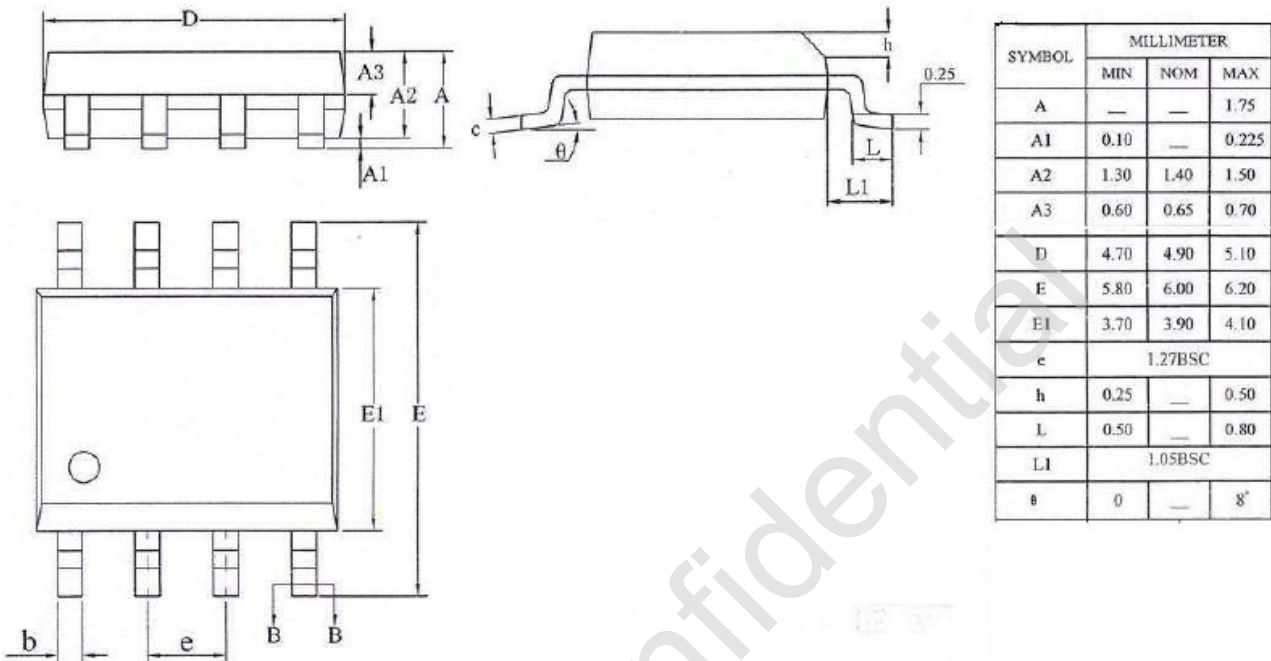
PRODUCT NAME: XT2114A for SOP8

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ABYYXX: AB product information, YYXX is production time

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PACKAGE INFORMATION

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0	—	8°

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end.

Dimension E1 does not include inter-lead flash or protrusion. Inter-lead flash or protrusion shall not exceed 0.25 mm per side.

D and E1 dimensions are determined at datum H. The package top may be smaller than the package bottom.

Dimensions D and E1 are determined at the outer most extremes of the plastic boxy exclusive of mold flash, tie bar burrs, gate burrs and inter-lead flash, but including any mismatch between the top and bottom of the plastic body

Disclaimer

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