# XT410X Emergency Detecting Controller

## Features

- Active Power Factor Correction
- PF>0.9 , THD<15% with high line input
- Built-in HV Power Supply Circuit
- Internal 600V/650V Power MOSFET
- No VDD, COMP Capacitor Design
- Programmable OVP
- QR Operation Mode for High Efficiency
- High Output Current Accuracy<±3%
- Ultra-low Operation Current
- Good Line and Load Regulation
- Built-in Protections:
  - Output Over Voltage Protection (OVP)
  - Cycle by Cycle Current Limit (OCP)
  - Leading Edge Blanking (LEB)
  - LED Open and Short Protection
  - Line OVP
- Thermal Fold-back (OTP)
- Package Available with SOP-7, DIP-7

## Applications

- LED Driver

## Description

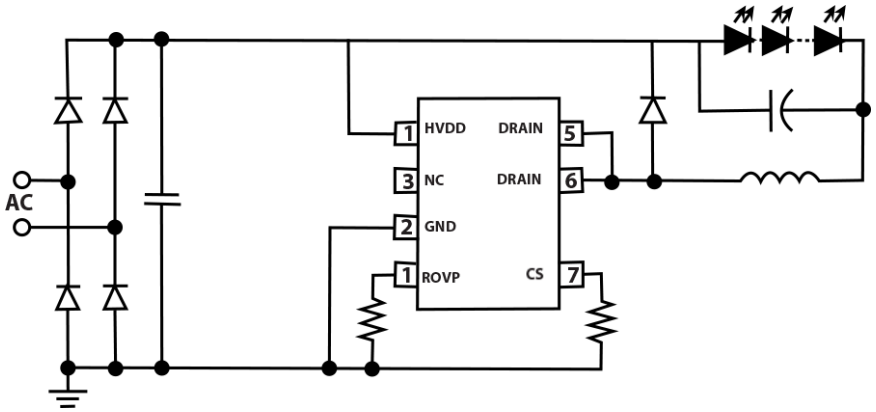
XT410X is a family of highly integrated Constant Current LED power switch. The IC utilizes Quasi-Resonant (QR) Buck topology with active PFC control for high PF, low THD, and high efficiency.

XT410X integrates internal demagnetization detection circuit and 650V/600V power MOSFET with high voltage startup, which eliminates auxiliary winding for power supply and demagnetization and simplifies the design and production cost of the system. Additionally, the system surge performance is also optimized in XT410X to pass 2.5kV surge level with minimum system cost. The IC adopts accurate current sensing, close loop constant current control to achieve high precision CC control with excellent line and load regulation.

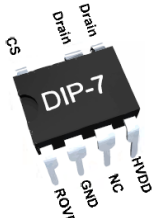
XT410X integrates functions and protections of Cycle-by-cycle Current Limiting (OCP), Thermal Fold-back (OTP), Line OVP, Output Over Voltage Protection (OVP), LED Open/Short Protection, etc.



## Typical application(non-isolated circuit)



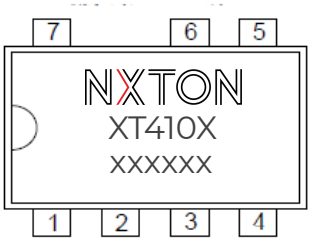
## Pin Configuration



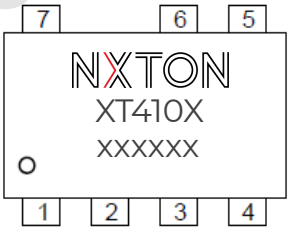

DIP-7


SOP-7

## Marking Information




DIP-7




SOP-7

## Output Power Table

| Part Number | Package | Maximum Output Current (176-265 Vac) | |
|---|---|---|---|
| | | 36V output | 72V output |
| XT4108A2 | SOP-7 | 150mA | 110mA |
| XT4101A2 | SOP-7 | 200mA | 130mA |
| XT4102A2 | SOP-7 | 300mA | 240mA |
| XT4103A2 | SOP-7 | 400mA | 270mA |
| XT4103B2 | DIP-7 | 400mA | 270mA |

**Note: Maximum output power is constrained by IC maximum Junction Temperature and determined by ambient temperature and PCB. The system actual maximum output power is determined by the test.**

## Pin Description

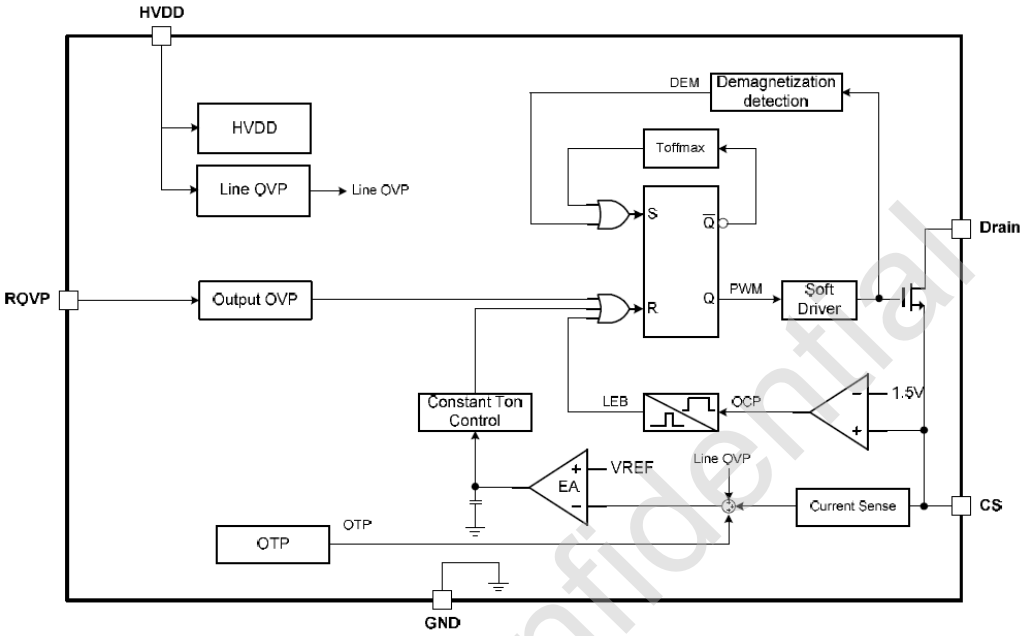
| Pin Number | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | ROVP | I | Output OVP adjustment pin. Connecting a resistor to GND can continuously adjust the OVP point. When Rovp<50kΩ, the system is closed. |
| 2 | GND | P | IC Ground Reference Pin |
| 3 | NC | | Left floating in use |
| 4 | HVDD | P | IC HV Supply Pin |
| 5, 6 | Drain | O | Internal power MOSFET Drain pin |
| 7 | CS | I | Internal power MOSFET Source and current sampling pin |



## Ordering Information

| Part Number | Description |
|---|---|
| XT4108A2 | SOP-7, Pb free in T&R, 4000Pcs/Reel |
| XT4101A2 | SOP-7, Pb free in T&R, 4000Pcs/Reel |
| XT4102A2 | SOP-7, Pb free in T&R, 4000Pcs/Reel |
| XT4103A2 | SOP-7, Pb free in T&R, 4000Pcs/Reel |
| XT4103B2 | DIP-7, Pb free in T&R, 50Pcs/Tube |

## Block Diagram




## Absolute Maximum Ratings (Note 1)

| Part Number | Value | Unit |
|---|---|---|
| HVDD Voltage | -0.3 to 650 | V |
| Drain Voltage | 0.3 to 650 | V |
| CS, ROVP Voltage | -0.3 to 7 | V |
| PDmax, Power dissipation @TA=50°C (SOP-7) (Note2) | 0.6 | W |
| θJA, Thermal Resistance---Junction to Ambient (SOP-7) | 165 | °C/W |
| PDmax, Power dissipation @TA=50°C (DIP-7) (Note2) | 0.9 | W |
| Package Thermal Resistance---Junction to Ambient (DIP-7) | 105 | °C/W |
| Maximum Junction Temperature | 150 | °C |
| Storage Temperature Range | -65 to 150 | °C |
| Lead Temperature (Soldering, 10sec.) | 260 | °C |
| ESD Capability, HBM (Human Body Model) | 3 | kV |

## Recommended Operation Conditions

| Parameter | Value | Unit |
|---|---|---|
| Operating Junction Temperature | -40 to 125 | °C |

## Electrical Characteristics (Ta = 25℃, if not otherwise noted)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|---|
| **Supply Voltage Section (HVDD Pin)** | | | | | | |
| $I_{HVDD\_ST}$ | Start-up current into VDD pin | HVDD< HVDD_ON | 0.8 | 1.4 | 2.0 | mA |
| $I_{HVDD\_ST}$ | Operation Current | Fsw=7kHz | 120 | 220 | 250 | uA |
| $HVDD_{\_ON}$ | HVDD Startup Voltage | | 13 | 15.5 | 17 | V |
| $HVDD_{\_OFF}$ | HVDD Under Voltage Lockout Enter | | 4.8 | 5.8 | 6.8 | V |
| **Timing Section** | | | | | | |
| $T_{DEM\_BLANK}$ | Demagnetization Detection blanking Time | (Note 3) | 0.8 | 1.4 | 2.0 | us |
| $T_{ON\_MAX}$ | Maximum ON Time | (Note 3) | 4.9 | 5.2 | 5.5 | us |
| $T_{OFF\_MAX}$ | Maximum OFF Time | | 100 | 140 | 180 | us |
| $F_{SW\_MAX}$ | Maximum Switching Frequency | | | 125 | | kHz |
| **Current Sense Input Section (CS Pin)** | | | | | | |
| $V_{CC\_REF}$ | Internal Reference for CC Loop Regulation | | 196 | 200 | 204 | mV |
| $T_{LEB}$ | OCP Leading Edge Blanking Time | | | 500 | | ns |
| $V_{CS\_MAX}$ | Current Limiting Threshold | | 1.4 | 1.5 | 1.6 | V |
| $T_{D\_OC}$ | Over Current Detection and Control Delay | | | 150 | | ns |
| **Line OVP** | | | | | | |
| | Line OVP (AC RMS value) | | 290 | 310 | 330 | V |
| **Over Temperature Protection** | | | | | | |
| $T_{SD}$ | Thermal Foldback Trigger Point | (Note 3) | | 155 | | °C |

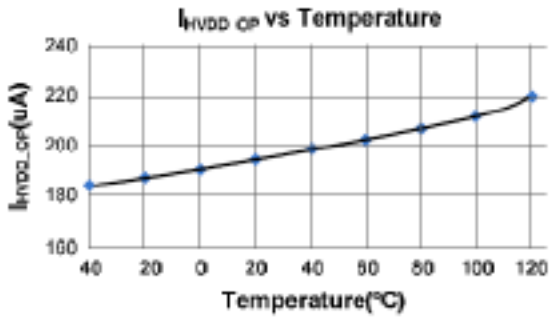
| Supply Voltage Section (HVDD Pin) | | | | | | |
|---|---|---|---|---|---|---|
| $V_{BR}$ | Power MOSFET Drain Source Breakdown Voltage | | | 650 | | V |
| $R_{dson}$ | Static Drain-Source On Resistance | XT4108A2 | | 13 | | Ω |
| | | XT4101A2 | | 8.5 | | Ω |
| | | XT4102A2 | | 4.5 | | Ω |
| | | XT4103A2 | | 2.4 | | Ω |
| Id | MOS Saturation Current[5)] | XT4108A2 | | 0.8 | | A |
| | | XT4101A2 | | 1 | | A |
| | | XT4102A2 | | 2 | | A |
| | | XT4103A2 | | 3 | | A |

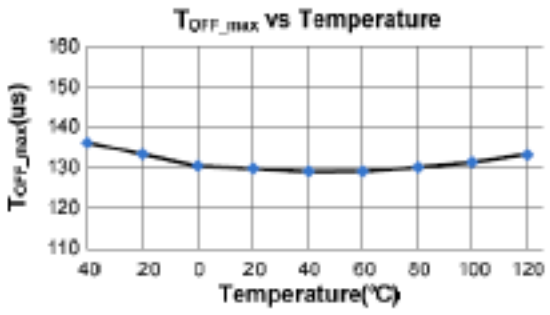
**Note 1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Expo sure to maximum rating conditions for extended periods may remain possibility to affect device reliability.**

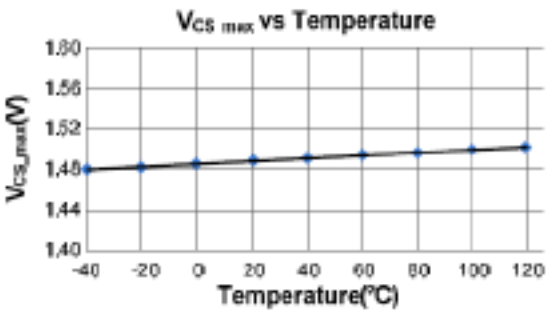
**Note 2. Maximum power dissipation** PDmax= (TJmax-TA)/θJA. **As ambient temperature rises, PDmax will decrease.**

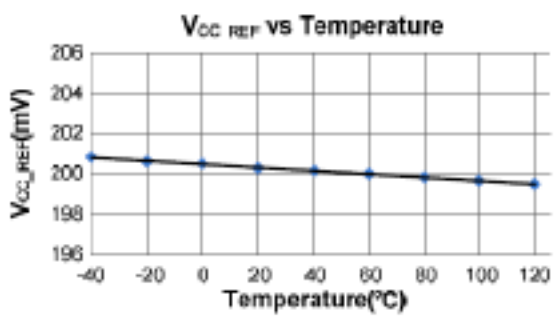
**Note 3. Guaranteed by the design.**

## Characterization Plots



## Operation Description

XT410X is a highly integrated power switch with constant current (CC) control for LED lighting applications. The IC utilizes Quasi-Resonant (QR) Buck topology with active PFC control for high PF, low THD, and high efficiency. XT410X integrates internal loop compensation capacitance (COMP capacitance) and VDD capacitance and supports for non auxiliary winding design. Output OVP voltage is continuously adjustable. The system cost can be minimized.

## System Start-Up Operation

After system power up, a digital counter is enabled. When 60ms had been counted, IC starts to switch at the lowest frequency, and then the output current slowly rises to the design value.

## Constant Current (CC) Control

XT410X samples the peak inductor current in each switching cycle to be as the CC loop feedback, and the high accurate output current can be realized with a high accurate current

$$I_{CC\_OUT}\,(mA) = \frac{V_{CC\_REF}}{R_{CS}} = \frac{200mV}{R_{CS}\,(\Omega)}$$

In the equation above,

Rcs--- the sensing resistor connected between CS and GND.

When AC input voltage drops, Ton will increase. When Ton reaches Ton_max, the output current will drop to limit IC temperature. The inductor can be set to adjust Ton and the curve. At the same time, in order to ensure the reliability of the system under high Vac, when Vac exceeds 310Vac, the output current will decrease. The output current curve vs. Vac is shown in Fig.1.

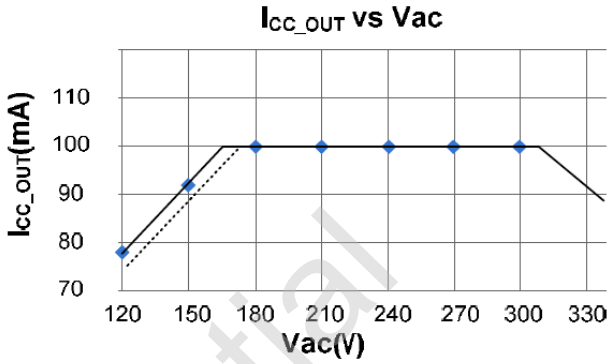



Fig.1

## Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by MOSFET parasitic capacitance and freewheeling rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading-edge blanking circuit is built in. During this blanking period (typically 500ns), the PWM comparator is disabled and cannot switch off the gate driver.

## Demagnetization Detection

XT410X integrates internal demagnetization detection circuit which eliminates the auxiliary winding and simplifies the design cost of the system.

## Timing Control

In XT410X, a minimum blanking time (typically 0.7us) is implemented to suppress ringing when the power MOSFET is off. Meanwhile the maximum OFF time in XT410X is typically 140us.The chip also integrates maximum frequency clamping function (typically 125 kHz) to achieve good EMI performance.

## Output Over Voltage Protection (OVP)

XT410X is integrated proprietary OVP control scheme, and the output over voltage can be programmed by the ROVP. The output over voltage
is determined by:

$$V_{OVP}(V) \approx \frac{2.62 \times 10^{10} \times L_P}{R_{OVP} \times R_{CS}}$$

where:
Lp---Inductance in H.
Rcs---current sense resistor in Ω
Rovp---the resistor connected between Rovp and GND, in Ω.

## Auto-Restart LED Open Protection

In the event of LED open circuit condition/output OVP protection, the IC enters auto-restart mode, wherein the power MOSFET is disabled and a digital counter is enabled. When 250ms had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above-mentioned process.

## On Chip Thermal Fold-back (OTP)

XT410X integrates thermal fold-back function. When the IC temperature is over 155oC, the system output regulation current is gradually reduced, as shown in Fig.2. Thus, the output power and thermal dissipation are also reduced. In this way, the system temperature is limited and system reliability is also improved.

## Soft Totem-Pole Gate Driver

XT410X has a soft totem-pole gate driver with optimized EMI performance.

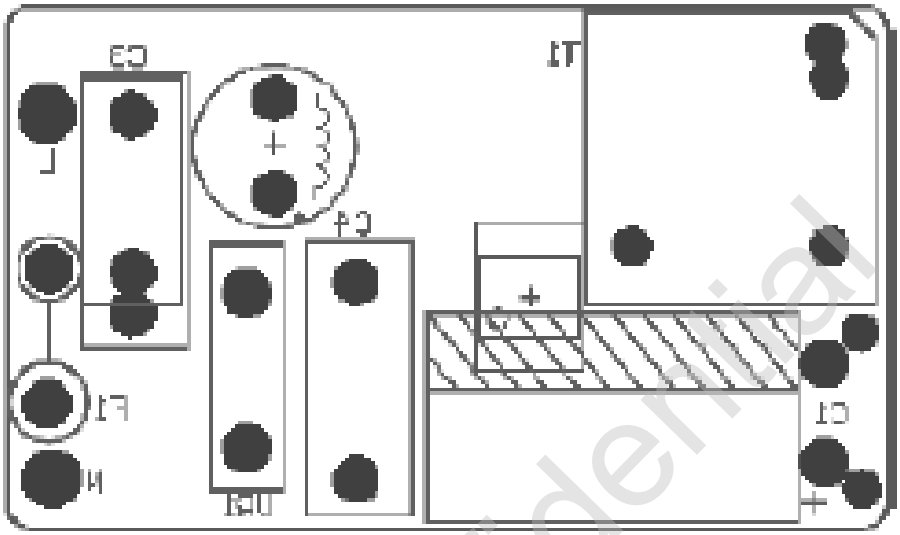
## PCB Layout Guidelines

PCB layout is very important for reliable operation. Please follow guideline to optimize performance.

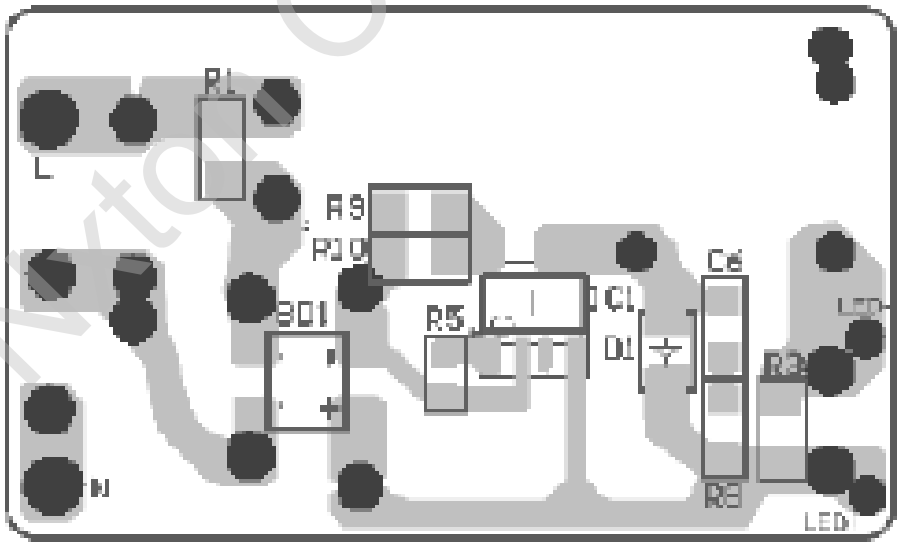
1. The area of main power switching loop should be as small as possible to reduce the EMI radiation, such as the inductor charging loop consisted of the EMI filter capacitor, output capacitor, inductor and IC; the inductor discharging loop consisted of the inductor, freewheeling diode and output capacitor.

2. Use single-point grounding. IC ground and other small signals ground should be connected to terminal ground point, the current sampling resistor ground. And the trace should be as short as possible.

3. Increase the copper area of the Drain pin to improve thermal performance. But too much copper area will worsen EMI performance.

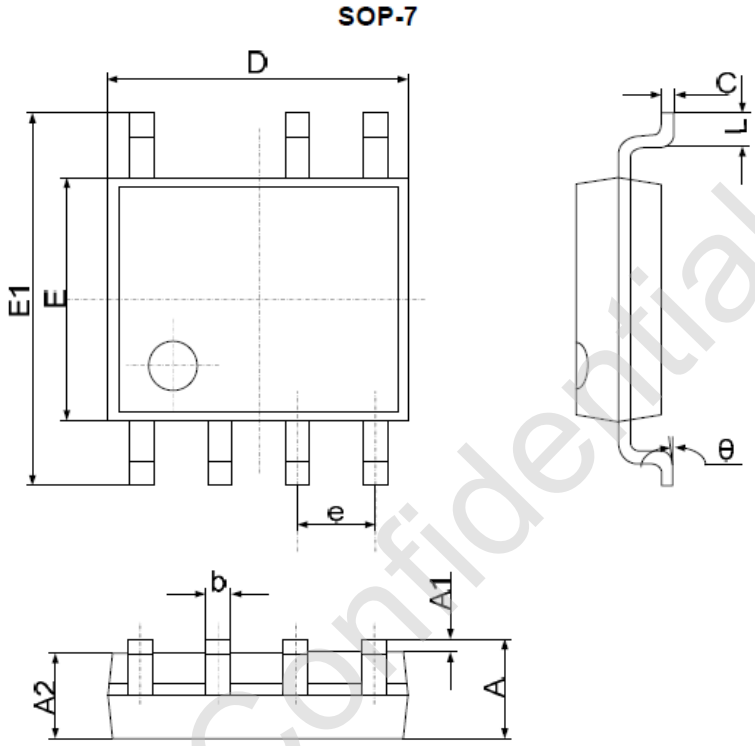


Top layout



Bottom layout

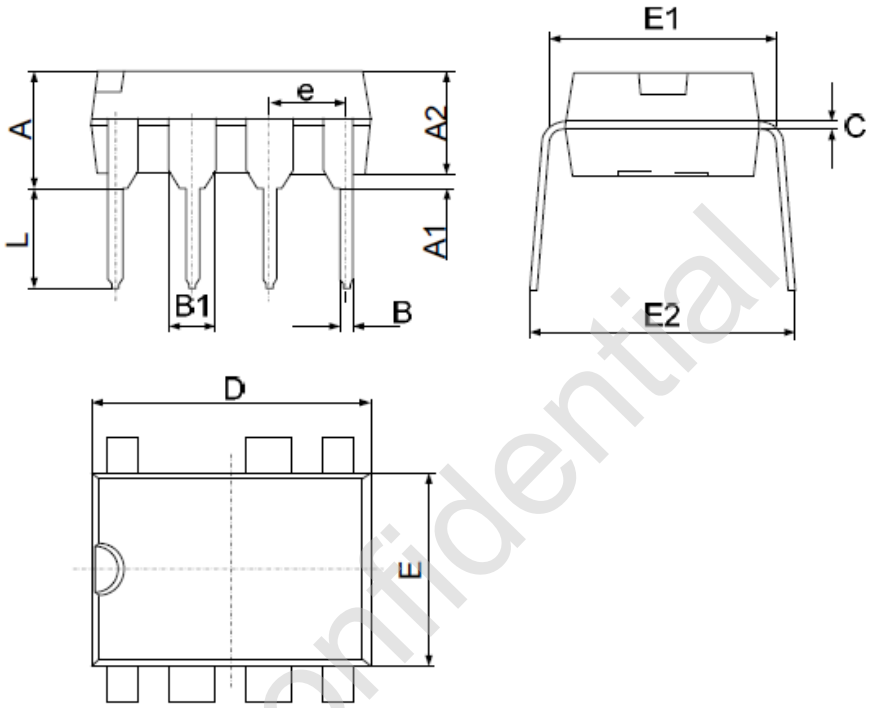
## Package Dimension




| Symbol | Dimensions in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.006 |
| D | 4.700 | 5.100 | 0.185 | 0.006 |
| E | 3.800 | 4.000 | 0.150 | 0.244 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 (BSC) | | 0.050 (BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| e | 0° | 8° | 0° | 8° |

## Package Dimension (Continued)

DIP-7




| Symbol | Dimensions in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 3.710 | 1.750 | 0.146 | 0.170 |
| A1 | 0.510 | 0.250 | 0.020 | |
| A2 | 3.200 | 1.550 | 0.126 | 0.142 |
| B | 0.380 | 0.510 | 0.015 | 0.022 |
| B1 | 1.524 (BSC) | | 0.060 (BSC) | |
| C | 0.204 | 5.100 | 0.008 | 0.014 |
| D | 9.000 | 4.000 | 0.354 | 0.370 |
| E | 6.200 | 6.200 | 0.244 | 0.260 |
| E1 | 7.320 | | 0.288 | 0.312 |
| e | 2.540 (BSC) | | 0.100 (BSC) | |
| L | 3.000 | 8° | 0.118 | 0.142 |
| E2 | 8.400 | 9.000 | 0.331 | 0.354 |

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